ABSTRACT OF THE DISCLOSURE

An INVSRC node and a SAREF node are previously precharged. After a potential on a bit line is reset, the bit line (BLS node) is precharged. In this event, a clamp MOS transistor in a sense amplifier is in ON state, and an SA node is also precharged simultaneously. A precharge level is set to a value lower than a threshold voltage of an inverter. Subsequently, when SAEN transitions to "H," a sense operation is performed. For reading data "0," the SA node is rapidly increased to Vdd. For reading data "1," the SA node slowly approaches to Vss. A change in the potential at the SA node is detected by the inverter.